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Review Article

Energy Dissipation and Transport in Nanoscale Devices

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ABSTRACT

Understanding energy dissipation and transport in nanoscale structures is of great importance for the design of energy-efficient circuits and energy-conversion systems. This is also a rich domain for fundamental discoveries at the intersection of electron, lattice (phonon), and optical (photon) interactions. This review presents recent progress in understanding and manipulation of energy dissipation and transport in nanoscale solid-state structures. First, the landscape of power usage from nanoscale transistors (~10^{-8} W) to massive data centers (~10^9 W) is surveyed. Then, focus is given to energy dissipation in nanoscale circuits, silicon transistors, carbon nanostructures, and semiconductor nanowires. Concepts of steady-state and transient thermal transport are also reviewed in the context of nanoscale devices with sub-nanosecond switching times. Finally, recent directions regarding energy transport are reviewed, including electrical and thermal conductivity of nanostructures, thermal rectification, and the role of ubiquitous material interfaces.

KEYWORDS

Nanowire, nanotube, interface, thermal transport, rectification, thermoelectric, power dissipation

1. Introduction

Some of the greatest challenges of modern society are related to energy consumption, dissipation, and waste. Among these, present and future technologies based on nanoscale materials and devices hold great potential for improved energy conservation, conversion, or harvesting. A prominent example is that of integrated electronics, where power dissipation issues have recently become one of its greatest challenges. Power dissipation limits the performance of electronics from handheld devices (~10^{-3} W) to massive data centers (~10^9 W), all primarily based on silicon micro/nano-technology. Put together, the energy use of the United States information technology (IT) infrastructure is currently in excess of 20 GW, or 5%–10% of our national electricity budget, with an approximate breakdown as shown in Figs. 1(c) and 1(d) [1]. Importantly, the figures for data center energy consumption have doubled in five recent years, with waste heat requiring drastic cooling solutions (Fig. 1(c)). Such challenges are also evident at the individual micro-processor (CPU) level, where the race to increase operating frequency beyond a few GHz recently stopped when typical dissipated power reached 100 W/cm^2 (Fig. 1(b)), an order of magnitude higher than a typical hot plate [2]. Such electronic power and thermal challenges have negative impacts in areas from massive database servers to new applications like wearable devices, medical instrumentation, or
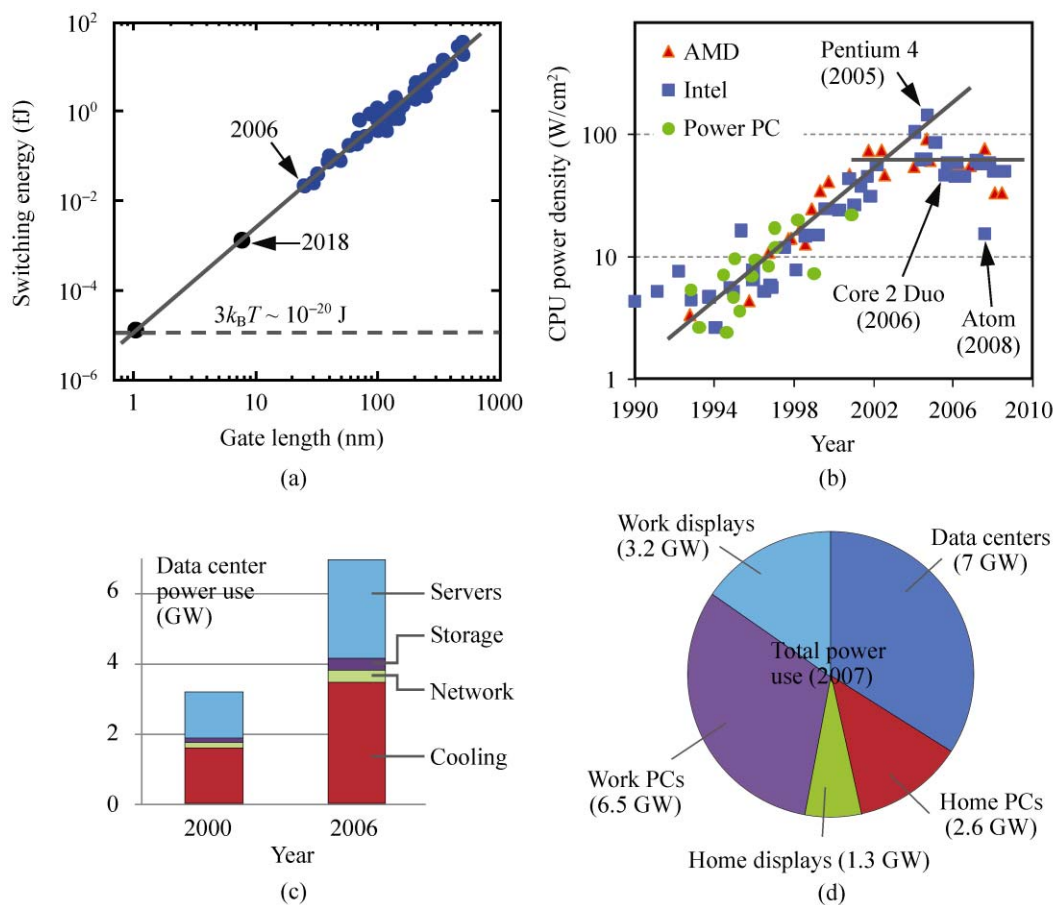
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Figure 1 Energy and power dissipation from transistors, to CPUs, to data centers. (a) Switching energy of modern silicon transistors is still over 1000× higher than fundamental physical limits, but on a trend toward them [3]. (b) Near-exponential increase of CPU power density in recent decades has flattened with the introduction of multi-core CPUs (solid lines show approximate trends); by comparison, the power density on the surface of the sun is approximately 6000 W/cm² [2]. (c) Data center power use in the U. S. doubled in six years, with an extremely large proportion devoted to cooling. (d) Approximate breakdown of total power used by digital electronics in the U. S., where data are available [1, 6, 8]

portable electronics. In the latter situations, there is a basic trade-off between the available functionality and the need to carry heavy batteries to power it.

Despite tremendous progress over the past three decades, modern silicon transistors are still over three orders of magnitude (>1000×) more energy inefficient than fundamental physical limits, as shown in Fig. 1(a). These limits have been estimated as approximately $3k_BT \approx 10^{-20}$ J at room temperature for a binary switch with a single electron and energy level separation k_BT, where k_B is the Boltzmann constant and T is the absolute temperature [3]. In the average modern microprocessor the dissipated power is due, in approximately equal parts, to both leakage (or "sleep") power and active (dynamic) switching power [4], as detailed in Section 2. Power dissipation

is compounded at the system level, where each CPU Watt demands approximately 1.5× more for the supply, PC board, and case cooling [1]. Such power (mis)use is even more evident in systems built on otherwise power-efficient processors, e.g., in the case of the Intel Atom N270 (2.5 W power use) which is typically paired up with the Intel 945GSE chipset (11.8 W power use) [5]. At the other extreme, data centers require 50%–100% additional energy for cooling (Fig. 1(c)), which is now the most important factor limiting their performance, not the hardware itself.

If present growth trends are maintained, data center and overall electronics power use could reach one third of total U. S. consumption by 2025 [1]. Worldwide, the growth trends could be even steeper, given that technologically developed regions such as the U. S.,

Western Europe, and Japan currently account for 58% of the world's computers, but only 15% of the world population [6]. Such energy challenges for the electronics infrastructure stem not only from the power supply side which calls for new energy sources, efficient batteries, or thermoelectrics, but also from the demand side, i.e., the need for more energy-efficient computing devices. To put it in financial terms, data centers consumed more than 7 GW or $4.5 billion in 2006 (Fig. 1(c)) [1]. The estimated 108 million PCs in offices across the U. S. had an annual energy cost of $4.2 billion in 2008 [6]. More troubling, the amount of equivalent CO_2 emissions generated is approximately equivalent to that of 5 million cars, comparable to the entire state of Maryland.

In fact, such estimates are likely to be conservative, missing the power consumed by routers, networks, and the internet backbone where detailed studies are not available (however, a thought-provoking study of energy consumption by e-mail SPAM has recently been made [7]). Nevertheless, the overall negative impact of these trends (to predicted 2025 levels) on energy supplies, budgets, and the environment in terms of equivalent CO_2 emissions is staggering. Thus, breakthroughs in our understanding and improvement of energy efficiency in nanoelectronics will also have a global effect, impacting the entire structure of modern society.

On a broader scale, just over half the man-made energy in the world is wasted as heat (10^{13} W), from power plants and factories to car engines and the power bricks on our laptops. Efficiently reclaiming even a small percentage of such wasted heat would itself nearly satisfy the electricity needs of our planet [8]. The fundamental issues at hand are, in fact, a two-sided problem: on one side, there is a significant need for low-energy computing devices, which is perhaps the biggest challenge in micro/nanoelectronics today. On the other side there is the challenge of waste heat dissipation, guiding, or conversion into useful electricity.

This review discusses several aspects of the above, from the nanoscale circuits to device and materials perspective, as follows: Section 2 examines energy dissipation and optimization in nanoscale circuits, with focus on leakage vs. active power in nanoscale

technologies. Section 3 presents energy dissipation in nanoscale devices (e.g., silicon transistors) from the diffusive to the ballistic regime. Section 4 reviews concepts of steady-state and transient thermal transport in the context of nanoscale devices with sub-nanosecond switching times. Finally, recent directions regarding energy transport are reviewed, including electrical and thermal conductivity of carbon nanostructures and nanowires (Section 5), thermal rectification (Section 6), and the role of ubiquitous material interfaces (Section 7).

2. Energy dissipation in nanoscale circuits

Energy and power dissipation in nanoscale digital circuits is often described in the context of inverter activity, as shown in Fig. 2(a). Three components have been identified for digital power consumption: dynamic power used during switching for charging and discharging the inverter load, subthreshold leakage power, and short-circuit power (P_{SC}) [9]:

$$P = C_L V_{DD}^2 \alpha f + I_{leak} V_{DD} + P_{SC} \tag{1}$$

where α is the activity factor, C_L is the load capacitance, f is the clock frequency, and I_{leak} is the sub-threshold leakage current [10]. The short-circuit power is typically the smallest for well-designed circuits with equal rise and fall times [9, 11]. The leakage component, however, is a strong function of temperature T, and therefore implicitly dependent on the total power dissipated. Moreover, leakage current also scales exponentially with the voltage overdrive ($V_{GS} - V_T$) and is very sensitive to changes in threshold voltage:

$$I_{leak} = \frac{W}{L_{eff}} \mu_{eff} C_{ox} (m-1) \left(\frac{k_B T}{q} \right)^2 \exp\left(\frac{V_{GS} - V_T}{m k_B T / q} \right)$$
$$\cdot \left[1 - \exp\left(-\frac{V_{DS}}{k_B T / q} \right) \right] \tag{2}$$

where μ_{eff} is the effective mobility, C_{ox} the gate oxide capacitance, W and L_{eff} the effective channel width and length, T the absolute temperature, V_{DS} the drain voltage, V_{GS} the gate voltage, V_T the threshold voltage, q the elementary charge, and m the subthreshold body factor [11]. With (down) scaling of technology
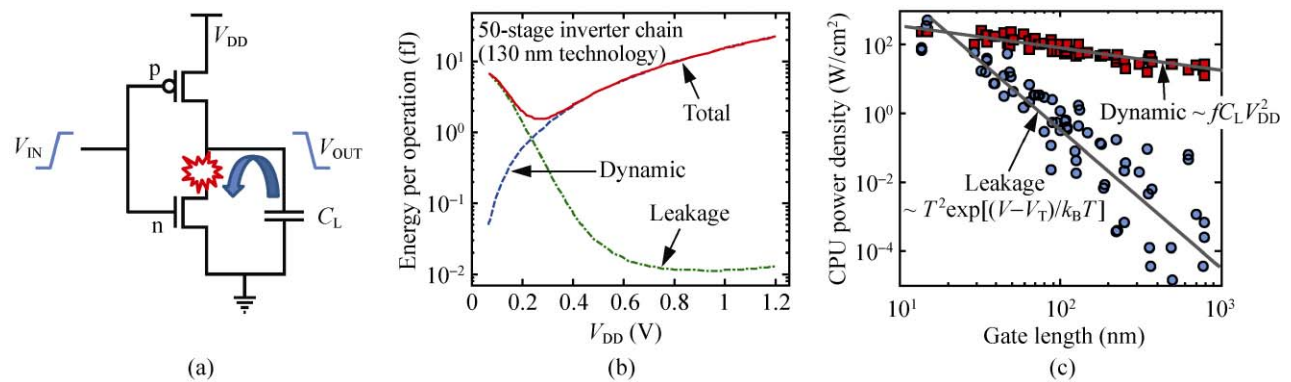
Figure 2 Power and energy dissipation in digital logic. (a) Schematic of a basic inverter. When the load capacitance C_L is discharged, its energy is dissipated in the drain of the n-FET as dynamic power ($\sim f C_L V_{DD}^2$). (b) Energy consumed per operation (a single clock period) by a 50-stage inverter chain displays a minimum with respect to supply voltage scaling [10, 11]. (c) Scaling of dynamic and leakage power density with CMOS technology [4]. In modern CPUs total power dissipation via leakage can be equal to or greater than the dynamic (active) switching power. Lines show scaling trends

dimensions and voltage, the role of sub-threshold leakage has become increasingly important, as shown by the trends in Figs. 2(b) and 2(c). This is due to a reduction in supply voltage V_{DD} without the ability to properly scale the threshold voltage, in addition to short-channel phenomena like drain induced barrier lowering (DIBL) [9].

An interesting trade-off becomes apparent if we compare the energy (rather than the power) dissipated by a simple digital circuit like an inverter chain, as shown in Fig. 2(b), here for a 130 nm technology with threshold voltage $V_T = 0.4$ V. Energy per operation is the more important metric for applications that are limited by battery life, such as mobile or medical devices. The dynamic energy, like the dynamic power, scales quadratically with the supply voltage V_{DD}. However, the leakage energy ($E_{leak} = I_{leak}V_{DD}t_d$) rises sharply as the supply voltage is reduced because the circuit delay (t_d) increases in sub-threshold ($V_{DD} \leqslant V_T$) operation. This raises an interesting point: for applications that are not concerned with maximum performance, the energy-optimal operation occurs in the sub-V_T regime for a given complementary metal oxide semiconductor (CMOS) technology, as shown in Fig. 2(b) [10, 11].

In applications that do seek optimal performance (such as desktop or server CPUs), leakage power dissipation has become significant, as illustrated in Fig. 2(c). Particularly, with respect to nanoscale devices with picosecond switching delays, Eq. (2) above merits a closer look, upon which several of its

shortcomings become evident. First, the expression was derived for three-dimensional diffusive transport across an energy barrier, whereas most nanoscale devices are one- or two-dimensional (the leakage current of a carbon nanotube transistor was recently derived in Ref. [12]). Second, leakage is strongly dependent on temperature, yet this itself is highly unsteady during transient digital switching. Typical electrical transients and inverter delays are of the order of 1–10 ps, whereas device thermal time constants are ~10 ns [13, 14]. Which temperature is used in computing the leakage current is an important choice, and using an average "junction temperature" as is often done [15] can lead to significant over- or under-estimates of the total leakage. Third, even if the thermal transients are properly accounted for in evaluating leakage during digital operation, the notion of temperature itself may need to be reconsidered when switching approaches the time scales of electron–phonon and phonon–phonon collisions (0.1–10 ps), leading to non-equilibrium conditions. Electrons scatter strongly with optical phonons (OP) in all materials and devices under consideration, and OP lifetimes are themselves of the order of 1–10 ps [16–20]. Optical phonons range from approximately 35 meV in Ge and GaAs, to 60 meV in silicon, and nearly 200 meV in carbon nanotubes and graphene [21], and hence the absorption of a single OP can lead to enough additional energy to immediately surpass the potential barrier in a metal oxide semiconductor field effect
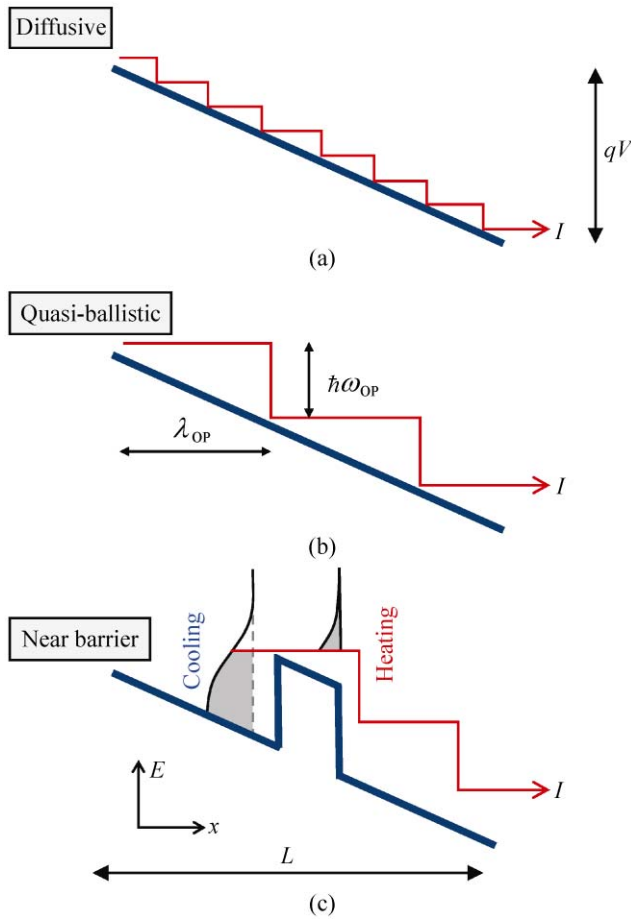
Figure 3 Schematic band diagrams and energy dissipation in (a) device under diffusive transport ($L \gg \lambda_{OP}$, $qV \gg \hbar\omega_{OP}$), (b) quasi-ballistic device ($L \sim \lambda_{OP}$, $qV \sim \hbar\omega_{OP}$), and (c) near an energy barrier. The barrier acts as an energy filter, resulting in lattice cooling to its left, and heating to its right (Peltier effect) [44, 45]. All cases assume a constant electric field

transistor (MOSFET)-like device (Fig. 3(c)). Recent results have also shown significant increase in band-to-band tunneling currents in carbon nanotubes due to optical phonon absorption [22]. As will be seen below, it is apparent that our present-day understanding and modeling of power dissipation in nanoscale circuits falls short of the recent advances made in nanoscale devices. This remains an area where significant progress remains to be made.

3. Energy dissipation in nanoscale devices

3.1 Diffusive, ballistic, and contacts

The most elementary approach for estimating the power dissipation of an electronic device is to express

it as the product of the current passing through and the voltage drop across it:

$$P_D = IV = I^2 R. \qquad (3)$$

This is the classical expression for a device under diffusive transport (subscript D), and the voltage drop excludes the device contacts (Fig. 3(a)). Hence, this equation must be applied with care in describing the power dissipated in a structure with relatively large contact resistance (R_C), e.g., a carbon nanotube or molecular device. The intrinsic device resistance also excludes the quantum contact resistance $R_0 = h/(Mq^2) \approx 25.8/M(\text{k}\Omega)$, where q is the elementary charge, h is Planck's constant, and M is the number of modes for electrical transport (e.g., $M = 4$ for single-walled carbon nanotubes, accounting for band degeneracy and spin) [23–26]. In large classical devices this can be ignored, as the presence of many transport modes ensures that R_0 is extremely small.

The expression above will overestimate the total power dissipated in a quasi-ballistic device, i.e., one with dimensions comparable to or shorter than the inelastic scattering length [27, 28], as schematically shown in Fig. 3(b). In this case, carriers gain energy comparable to the applied voltage ($E \approx qV$) but do not undergo enough inelastic scattering events to equilibrate and dissipate it to the lattice by the time they exit. In order to estimate dissipation in quasi-ballistic devices (subscript QB), we introduce the inelastic mean free path (MFP) λ_{OP}, typical for carrier scattering with high-energy optical phonons ($\hbar\omega_{OP} \approx 200$ eV in carbon nanotubes and ≈ 60 meV in silicon):

$$P_{QB} = \frac{\hbar\omega_{OP}}{q} \left(\frac{L}{L + \lambda_{OP}} \right) \frac{V}{R_0} \qquad (4)$$

where R_0 is the quantum of electrical resistance defined above, $\lambda_{OP} = L(\hbar\omega_{OP}/qV) + \lambda_0$, and λ_0 is the spontaneous OP emission MFP for carriers with energy $E > \hbar\omega_{OP}$ [29, 30] (for example, $\lambda_0 \approx 15d$ for a carbon nanotube with diameter d [31]). Here it is assumed that the current flowing through the device is limited by the inelastic scattering length, $I = (V/R_0)\lambda_{OP}/(L + \lambda_{OP})$ and that a carrier undergoes approximately L/λ_{OP} inelastic collisions within the device, each time losing an energy $\hbar\omega_{OP}$ to the lattice. In addition, the carrier is assumed

to relax to the bottom of its band immediately after the inelastic phonon emission event (Fig. 3(b)). Near the limit of zero temperature, an even sharper onset of power dissipation is expected, as soon as the applied voltage is large enough for carriers to emit a single phonon, $V \geqslant \hbar\omega_{OP}/q$, as shown for molecular junctions [32–35]. The expression above recovers the correct limit of power dissipation within a device in the ballistic limit ($P \rightarrow 0$ as $L \ll \lambda_{OP}$), although a more careful examination reveals that the scattering length itself depends on the phonon occupation and temperature at sufficiently high power levels. In this case, the electrical–thermal dissipation must be self-consistently solved, as in Refs. [30, 36]. Moreover, in quasi-ballistic transport hot carriers escape through the contact at higher voltage and a significant portion of the total power is dissipated there instead [37]. This can be interpreted as the difference between the input power and the power dissipated within the quasi-ballistic device (P_D–P_{QB} in Eq. (3) and (4) above).

A third example concerns heat dissipation during thermionic or tunneling transport across mesoscopic energy barriers, which are often encountered in transistors, diodes, heterojunctions, and device contacts (Fig. 3(c)). Such dissipative transport does not lend itself to a simple, analytic interpretation, but it has been examined with the non-equilibrium Green's functions (NEGF) approach [27, 38], by Monte Carlo simulations [39, 45], and the scattering matrix method [40]. A key feature of dissipation near barriers is the role of the energy barrier as a filter of the carrier distribution function, as schematically shown in Fig. 3(c). Carriers with higher energy have a greater transmission probability (either thermionic or tunneling) across the barrier, leading to a "cooler" carrier distribution to the left (uphill) of the barrier, and a "hotter" distribution to the right (downhill). This results in an effective cooling (negative heat dissipation) to the left, and heating of the lattice (positive heat dissipation) to the right of the barrier. This effect depends not only on the barrier shape and height, but also on the direction of the current flow. In addition, such asymmetric heating can also be observed at metal–semiconductor contacts [41, 42], at contact energy barriers between dissimilar semiconductors [43–45], and even at more subtle transitions between regions

with different densities of states (DOS). The latter is a thermoelectric effect recently observed in transport between monolayer and bilayer graphene [46] and is a result of hot carriers diffusing from regions of lower to higher DOS in order to maximize the entropy (also equivalent to the classical effect of a gas that cools as it expands).

3.2 Spatial distribution of energy dissipation

Returning in more detail to the case of diffusive transport (dimension $L \gg$ inelastic MFP), more sophisticated methods are needed to compute the *spatial* distribution of power dissipation, instead of the simple lumped result of Eq. (3). This is most often given by the drift-diffusion approach [47–50]:

$$P_V = \boldsymbol{J} \cdot \boldsymbol{E} + (R-G)(E_G + 3k_BT) \tag{5}$$

where $\boldsymbol{J}$ is the current density, $\boldsymbol{E}$ the electric field, $(R-G)$ is the net non-radiative recombination rate (recombination minus generation), E_G is the semiconductor band gap, and T is the lattice temperature. The factor $3k_BT$ arises when the average energy of an electron (hole) above (below) the conduction (valence) band is ~$3/2k_BT$. The result above is typically implemented as a finite-element simulation on a device grid. Note the notation of P_V (power density per unit volume, i.e., W/m³) vs. Eq. (3) above (total power in Watts). The total power dissipated can be recovered by integrating Eq. (5) over the device volume. The first term represents the Joule heating rate which is usually positive (power generation) as charge carriers move along the band structure under the influence of the electric field, giving up energy to the lattice. This equation may include higher order terms accounting for carrier drift along a temperature gradient or across a discontinuity in the band structure [43, 45, 48].

Unfortunately, this field-dependent method does not account for the microscopic nature of heat generation near a strongly peaked electric field region, such as in the drain of the transistor. Although electrons gain most of their energy at the location of the peak field, they travel several mean free paths before releasing it to the lattice, in decrements of (at most) the optical phonon energy. In silicon, the optical phonon energy is $\hbar\omega_{OP} \approx 60$ meV and in carbon nanotubes or graphene

it is approximately three times greater. Typical inelastic scattering mean free paths in both silicon and carbon nanostructures are of the order $\lambda_{OP} \approx 10$–50 nm [31]. The full electron energy relaxation length is thus even longer, i.e., several inelastic mean free paths. This is illustrated near a 20 nm wide energy barrier in silicon in Fig. 4, where the drift-diffusion approach cannot capture the delocalized nature of the power dissipation region.

An improvement is provided by the hydrodynamic approach, which introduces the electron temperature (T_e) and an average electron energy relaxation time (τ_{e-L}) [48]:

$$P_V = \frac{3}{2}\frac{k_B n(T_e - T_L)}{\tau_{e-L}} + (R-G)\left[E_G + \frac{3k_B}{2}(T_e + T_L)\right] \quad (6)$$

where n is the electron density and L denotes the lattice. The equation here is written for electrons as majority carriers, but the holes can be treated similarly. Unlike the drift-diffusion model, this approach is better suited for capturing transport near highly peaked electric fields. However, this suffers from the simplification of a single averaged carrier temperature and relaxation time, as scattering rates are strongly

energy-dependent [51]. Neither method gives information regarding the frequencies and wave vectors of phonons emitted. Such details are important because the emitted phonons have different velocities and widely varying contributions to heat transport [52–55] and device heating [56, 57].

The mechanism through which lattice self-heating occurs is that of electron scattering with phonons, and therefore a model which deliberately incorporates all scattering events will also capture such energy dissipation details. Thus, the Monte Carlo method [58] originally developed for studying hot electron effects [59], is also well-suited for computing a detailed picture of energy dissipation. This was the approach adopted in Refs. [60–64], where power dissipation was computed as a sum of all phonon emission minus all phonon absorption events:

$$P_V = \frac{n}{N_{sim}\Delta t}\sum\left(\hbar\omega_{ems} - \hbar\omega_{abs}\right) \quad (7)$$

where n is the real-space carrier density, N_{sim} is the number of simulated particles (e.g., 10 000 simulated particles could be used to describe 10^{19} cm^{-3} real-space concentration), and Δt is the time. This approach has
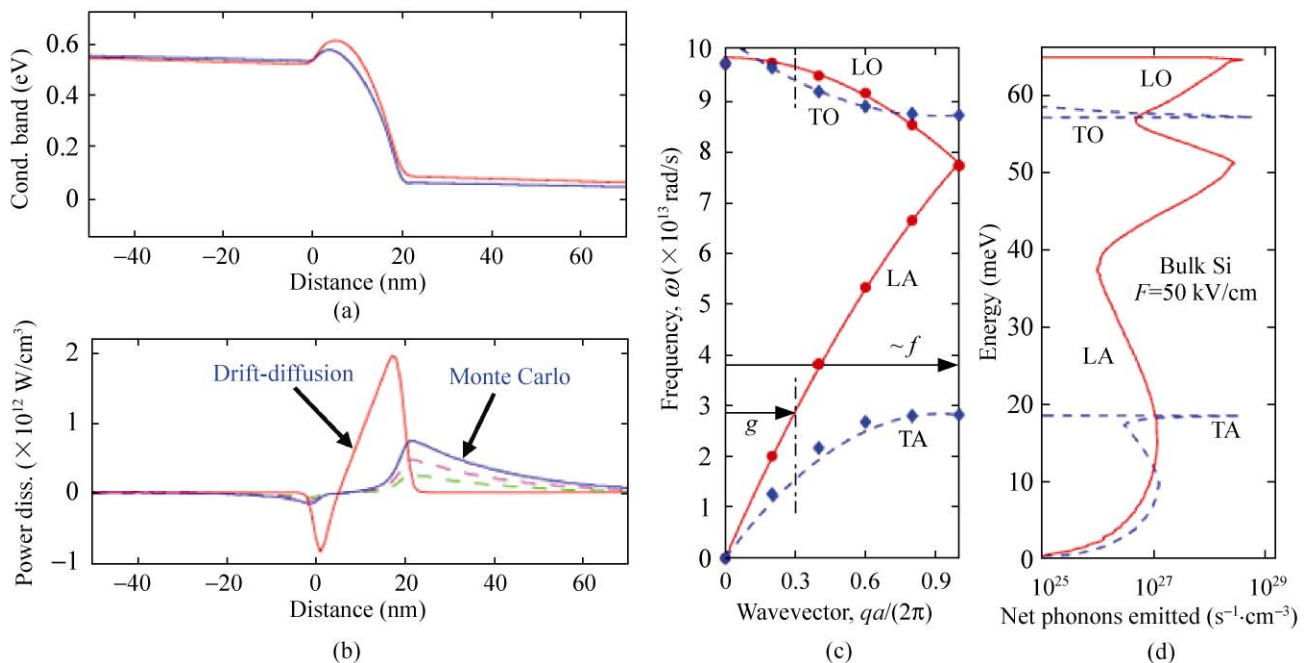

Figure 4 Computed spatial and phonon-resolved power dissipation in silicon. (a) Conduction (cond.) band diagram of a 20 nm wide energy barrier and (b) non-localized power dissipation (diss.) near it. Dashed lines represent optical (upper) and acoustic (lower) phonon emission computed with a Monte Carlo approach [51]. (c) Phonon dispersion in silicon and (d) corresponding phonon generation spectrum from Joule heating. Transverse modes are dashed lines, longitudinal modes are solid lines. Reproduced with permission from Ref. [60]. Copyright 2005 American Physical Society

been used to investigate phonon emission as a function of frequency and mode in silicon, as well as to study heat generation near a strongly peaked electric field in a realistic device geometry. Figure 4(b) shows the comparison between a classical drift-diffusion calculation and that of the Monte Carlo result. The former tends to overestimate the peak heat generation rate and predicts a narrower heat generation region, which follows the shape of the electric field. The Monte Carlo method suggests a broader heat generation domain extending inside the device drain, and chiefly limited by the electron-phonon scattering rate there.

The Monte Carlo approach also shows that heat generation in silicon is not evenly divided among phonon modes, but that acoustic phonon modes receive approximately 1/3 and optical phonons 2/3 of the energy dissipated, as shown in Fig. 4(d). More specifically, the longitudinal optical (LO) *g*-type phonon is responsible for approximately 60% of the total energy dissipation [60]. Optical phonons have group velocities below 1000 m/s, and are thus much slower than the Brillouin zone center acoustic phonons typically responsible for heat transport in silicon (group velocity 5000–9000 m/s). This non-equilibrium phonon generation can lead to an energy transfer bottleneck [56]. In other words, a significant non-equilibrium phonon population may build up, particularly for the *g*-type LO mode. The generation rates for the other phonon modes are either smaller or their DOS is larger (the DOS is proportional to the square of the phonon wave vector, which is largest at the edge of the Brillouin zone) and non-equilibrium effects are less significant.

The self-consistent study of Rowlette and Goodson [61] built on previous work by Pop [60] and Sinha [62], and coupled the Monte Carlo method for electron transport with a Boltzmann transport equation (BTE) approach for phonon transport. Rowlette found that while extremely high heat generation densities do exist in modern silicon devices (>10^{12} W/cm³), non-equilibrium hot phonon effects are strongly dependent on the phonon relaxation time. Available data points at an optical phonon lifetime $\tau \approx 0.4$–2 ps for optical phonons near the Brillouin zone center [18], but the phonons involved in electron scattering are the *g*- and *f*-type shown in Fig. 4(c), for which no experimental lifetimes are available. The discrepancy

between the LO phonon temperature computed with the self-consistent vs. the classical approach can be as high as 250% in the device drain, near the location of highest electric field [61]. However, the electron mobility is typically determined by the temperature and scattering mechanisms near the source of the channel in such quasi-ballistic devices [65], and does not appear to be strongly influenced by the additional LO population. Nevertheless, device reliability may ultimately be affected by such hot phonons, as suggested by a recent experimental study [66].

4. Thermal transport in nanoscale devices

4.1   Steady-state thermal resistance

While the previous sections focused on power dissipation in nanoscale devices and circuits, this section and the subsequent ones shift our attention to heat transport in and thermal spreading from nanoscale devices and materials. At the simplest level, heat dissipation from a lumped electronic device can be quantified by measuring its thermal resistance (R_{TH}) to the environment. This approach yields an average temperature rise of the device as:

$$\Delta T = P R_{TH} \qquad (8)$$

where P is the power (heat) dissipated in Watts. Note this is extremely similar to the electrical Ohm's law ($\Delta V = IR$), with temperature taking the role of voltage and power having the role of electric current flow. For instance, the thermal resistance to heat flow across a layer of thickness δ and cross-sectional area A is written analogously to its electrical resistance, as $R_{TH} = \delta/(kA)$, where k is the material thermal conductivity. As with the electrical conductance (resistance) quantum, there also exists an equivalent ballistic quantum of thermal conductance, which is directly proportional to absolute temperature, $G_0 = \pi^2 k_B^2 T/(3h)$ or approximately 0.28 nW/K near 300 K [67, 68]. By comparison, the thermal conductance of an individual single-walled carbon nanotube at room temperature has been measured to be 2.4 nW/K [69].

In practice, nanoscale and semiconductor devices take more varied shapes (Fig. 5), have many modes available for thermal transport, and interfaces or

three-dimensional heat spreading which make their analysis more difficult. The thermal resistance of many semiconductor devices has been measured through noise thermometry [70], gate electrode electrical resistance thermometry [71, 72], pulsed voltage measurements [13, 73], or an AC conductance method [14, 74–76]. Figure 5(a) presents a summary of such experimental data produced in the literature over the past nearly two decades, covering a wide range of device dimensions and technologies. A clear trend emerges, showing that device thermal resistance increases as a power law with reduced device dimensions, and is reaching values well above 10^5 K/W for device dimensions below 100 nm. Carbon nanotube (CNT) devices present a particularly interesting case, showing relatively high thermal resistance. This is due partly because they are usually measured on a relatively thick SiO_2 layer (50–300 nm), partly because of their much smaller "footprint" area (CNT diameter $d \ll$ any other typical device widths W), and partly to the thermal resistance at the CNT–SiO_2 interface [30, 77–79]. In other words, it is clear that the geometry, thermal conductivity of materials, and the thermal resistance of material interfaces play a significant role

in determining the thermal impedance of a nanoscale device.

To understand the scaling displayed in Fig. 5(a), consider the simplest case of a circular device with diameter D on the surface of a silicon wafer (of thickness $\gg D$). Its thermal resistance will scale as $R_{TH} = 1/(2k_{Si}D)$ as that of the spreading electrical resistance from a single circular contact [80]. This can be extended to a rectangular heat source (width W, length L) by replacing $D \approx (LW)^{1/2}$ and including additional three-dimensional heat spreading shape factors [71, 81]. This case is illustrated in Fig. 5(b), along with that of a cylindrical device (e.g., nanotube, nanowire). Several online tools are also available for quick, web-based spreading resistance calculations for various shapes and substrates [82]. Many other models of varying sophistication have been published, all of which reveal various inverse length and width dependencies [71, 72, 83, 84]. Naturally, the choice of such a model in practice depends on its complexity, and on the specific geometry of the device. Care must also be taken with the limiting cases $W \gg t_{ox}$ (one-dimensional heat flow through the underlying oxide) as opposed to d or $W \ll t_{ox}$ (three-dimensional spreading
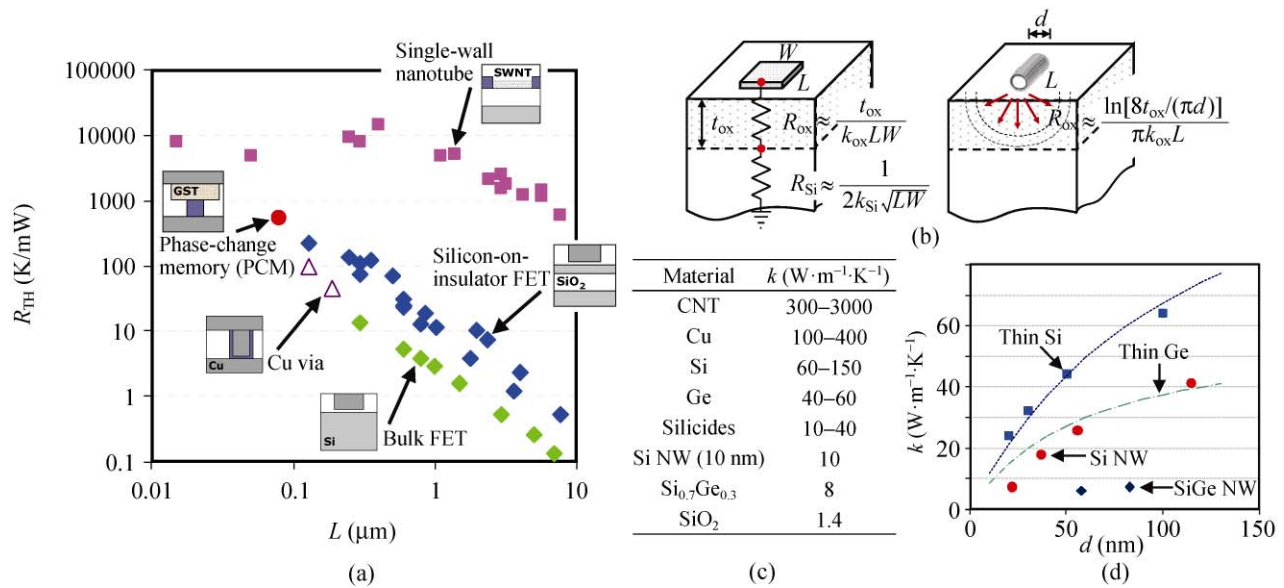

Figure 5 (a) Measured thermal resistance of individual devices [13, 14, 30, 70–78, 161].. Thermal resistance generally scales inversely with device size L and substrate thermal conductivity k. (b) Simple themal models for rectangular (assuming $W \gg t_{ox}$) and cylindrical devices (assuming $d \ll t_{ox}$) [30, 71, 72]. (c) Thermal conductivities at room temperature. Approximate ranges are given by grain boundary or impurity scattering, and by defects or wall number for CNT [69, 103, 162]. (d) Thermal conductivity data along thin films and nanowires (NW), showing strong decrease with nanowire diameter or film thickness due to phonon-boundary scattering [127, 132]. Dashed lines are simple models for Si and Ge [163]

into the oxide), the latter being the case for all nanotube, nanowire, and even graphene nanoribbon data [85] typically available. Finally, the thermal boundary resistance (TBR) at the interfaces between the devices and its environment can also be a limiting factor, as is the case with nanotubes [30, 86], phase-change memory devices [87, 88], and to some extent graphene transistors [89, 90]. The TBR in the latter case is approximately equivalent to the thermal resistance of 20–50 nm SiO_2 at room temperature, and makes relatively little contribution for the commonly used graphene samples on 300 nm SiO_2. However, to estimate heat dissipation from graphene with thinner dielectrics, the TBR must be included in series with the additional material thermal resistances in Fig. 5(b), at the interface between the device and its adjacent dielectric. More discussion on the TBR is provided in Section 7.

4.2   Transient heat conduction

The thermal resistance models mentioned above are sufficient for evaluating the steady-state behavior of semiconductor devices, i.e., relevant during *I–V* characterization, analog operation, or to estimate the average temperature rise owed to device leakage. However, an understanding of transient heat conduction is necessary for short duration pulsed operation, such as during digital switching [9] or electrostatic discharge (ESD) events [91].

To first order, the temperature rise of a pulse-heated volume can be obtained from the energy of the heating pulse (E) and the heat capacity (C) of the volume (V) being heated:

$$\Delta T\left(t_{\rm p}\right) \approx \frac{E}{CV} = \frac{Pt_{\rm p}}{CV} \qquad (9)$$

where $t_{\rm p}$ is the pulse duration and P is its power. For instance, during digital operation the duration of an inverter switching event is approximately $t_{\rm p} \approx$ 50–100 ps (or shorter), which is significantly less than the thermal time constant of most modern devices, $\tau \approx$ 10–100 ns [92]. This is near the "adiabatic limit", where the device can be thermally decoupled from its environment. In other words, while the device is ON there is little spread of the heated volume outside the area where the actual heating takes place

(here, the channel and drain of the transistor).

The approximation above holds only for heating pulses that are short enough not to cause any significant heating outside the device volume. For a pulse of duration $t_{\rm p}$ the temperature spread extends approximately $(\pi \alpha t_{\rm p})^{1/2}$ outside the directly heated device volume [93], where $\alpha = k/C$ is the heat diffusion coefficient and k is the thermal conductivity (Fig. 5(c)). For heating pulses of $t_{\rm p}$ = 50 ps this distance is of the order ~100 nm into silicon or germanium, and ~10 nm into adjacent SiO_2 layers (like the top passivation layer, or the buried oxide below silicon-on-insulator, i.e., SOI technology). For longer heating pulses $t_{\rm p} \gg$ 50 ps or device dimensions $D <$ 100 nm, we must take into account both the energy stored as temperature rise within the device and that in the surrounding dielectric (the heated volume of which expands as ~$t_{\rm p}^{1/2}$). In this case we can estimate [15, 94]:

$$\Delta T\left(t_{\rm p}\right) \approx \frac{P}{CV}\left(2\sqrt{\tau t_{\rm p}} - \tau\right) \qquad (10)$$

where $t_{\rm p} > \tau$ and $\tau = D^2/(4\pi\alpha)$ is the time constant associated with the minimum device dimension D. The expression above assumes the same heat capacity for both the device and its surrounding dielectric, which is a good approximation for Si and SiO_2 near room temperature ($C_{\rm Si} \approx C_{\rm ox} \approx$ 1.7 J·cm^{-3}·K^{-1}). Typical estimates of the temperature rise during digital switching have shown that this dynamic value does not exceed a few degrees (e.g., 5 K) for sub-micron device technologies [14, 92]. However, the exact value for devices in the 10 nm range is unknown, and will be highly dependent on the ultimate choice of device geometry, materials, and interfaces.

For longer time scales, comparable to or larger than the device thermal time constants, several models have been proposed [81, 84, 88, 94, 95]. These bridge the time range from the adiabatic limit to the steady-state operation of a device, and are typically based on a Green's functions solution of the heat diffusion equation. This approach is faster and offers more physical insight than solutions based on finite-element (FE) solvers. The disadvantage of such methods vs. the FE approach is their applicability to only a limited

range of geometries, like a heated sphere, infinite cylinder or rectangular parallelepiped, and not taking into account the full geometry and diverse materials making up a modern semiconductor device.

Finally, for time scales or power pulses longer than the thermal diffusion time through the silicon wafer backside (~0.3 ms assuming a 500 μm thick wafer) the problem returns to a simpler one of steady-state temperature rise. This was the case described in Section 4.1, and the temperature rise can be again obtained simply as a product of the (average) power input and that of the overall thermal resistance, $\Delta T = PR_{\text{TH}}$.

5. Energy transport in nanotubes, graphene, and nanowires

5.1 Carbon nanotubes and graphene

Carbon nanotubes (CNTs) and more recently graphene have emerged as new materials for electronics [96–98]. Graphene is a monolayer of graphite, a single sheet of hexagonally-arranged carbon atoms (Fig. 6(a)), first isolated five years ago [99]. Carbon nanotubes are cylindrical molecules with diameters ~1–3 nm, essentially "rolled-up" graphene obtained from chemical reactions [100]. Both materials have generated considerable interest because they demonstrate high mobility, thermal conductivity, and (particularly for graphene) the potential for integration with planar CMOS. Their excellent electrical and thermal properties make them especially attractive for energy efficient nanoelectronics. From this point of view, compared to traditional silicon, devices based on carbon nanomaterials benefit from:

(1) symmetric energy bands (Fig. 6(b)) and equal electron/hole mobility, both 10–100 times higher than silicon [101, 102], indicating less scattering and lower power dissipation.

(2) strong sp² bonds leading to thermal conductivity ~10–20 times higher than silicon, 5–10 times higher than copper, and comparable to that of isotopically pure diamond [69, 103, 104].

(3) optical phonon (OP) energies three times higher than in silicon (~180 meV vs. ~60 meV, Fig. 6(c)), suggesting they are less occupied and less likely to scatter electrons at low fields and near room temperature [30].

Energy dissipation in CNTs and graphene occurs when electric fields accelerate charge carriers (electrons or holes), which then scatter with lattice phonons. It has been generally assumed that the strongest high-field relaxation mechanism is that with OPs, which have high energy $\hbar\omega_{\text{OP}} \approx 160$–200 meV [105–109]. For instance, heating and scattering with hot OPs is responsible for the negative differential conductance observed in suspended CNTs [36, 110–112], as shown in Fig. 7(d). For substrate-supported CNTs, theoretical work has suggested that energy dissipation could also occur directly with "remote" polar surface-optical (SO) phonon modes in the substrate, bypassing
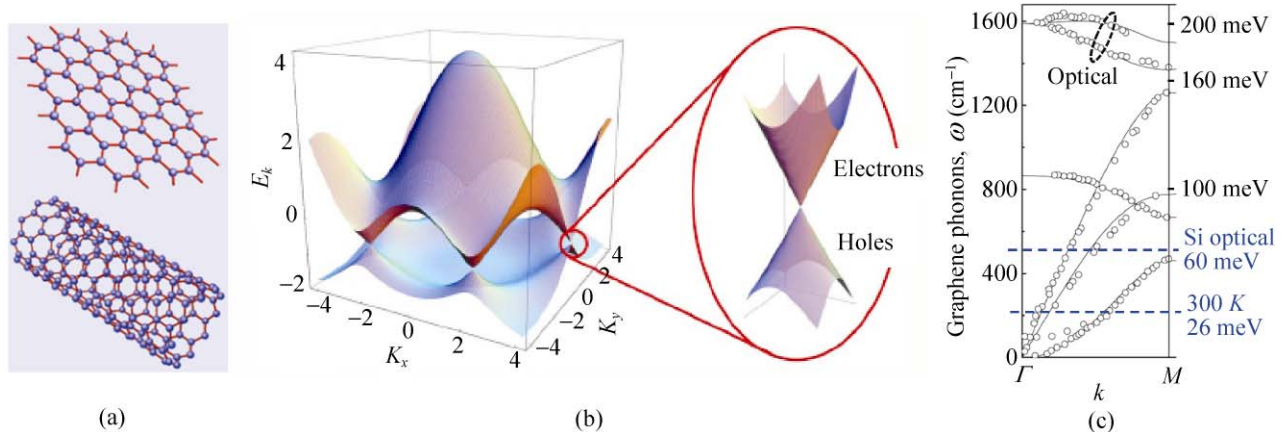

Figure 6 (a) Lattice structure of graphene (top) and carbon nanotubes (bottom) [96]. (b) Energy dispersion in graphene. Right: energy bands close to the Dirac point show linear dispersion. Reproduced with permission from Ref. [164]. Copyright 2009 American Physical Society. (c) Phonon dispersion in graphene, showing optical phonon energy much greater than that in silicon, and much above the room temperature energy ($k_B T \sim 26$ meV). Modified and reproduced with permission from Ref. [165]. Copyright 2005 John Wiley and Sons

heating of the CNT [113, 114] (Fig. 7(b)). For example, the lowest SO phonons of several substrates have energies of approximately $\hbar\omega_{SO} \approx 48$ meV for Al_2O_3, 56 meV for SiO_2, and 81 meV for AlN [55]. These are significantly lower than the CNT optical phonons, and may allow the device to directly dissipate part of its energy into the nearby insulator. A similar result has also been predicted for graphene on insulators like SiO_2 or HfO_2 [115], and is well known in silicon inversion layers with high-κ dielectrics [55, 116]. However, evidence of direct energy dissipation with substrate phonons is presently lacking, perhaps in large part due to the expected exponential dependence of electron-SO coupling on the CNT-substrate distance [114]. Thus, surface roughness, which for CNTs and graphene can be of the order of the device "thickness,"

or adsorbed water and impurities could significantly mask the electron-SO coupling. Nevertheless, a few studies do reveal phonon non-equilibrium in CNTs [86] and a reduction of mobility in graphene [102, 117] which have been attributed to scattering with substrate SO phonons. Interestingly, although not yet confirmed, a trade-off appears to exist between the SO scattering effect on mobility and power dissipation. Soft, low-energy SO phonons limit mobility, but at the same time enhance direct CNT cooling with the substrate.

More can be understood about energy dissipation and transport in one-dimensional CNT and graphene devices by measuring their temperature during Joule heating by electrical current flow. Assuming a uniform heating rate per unit length $P/L \approx I^2(R-R_C)/L$, where R
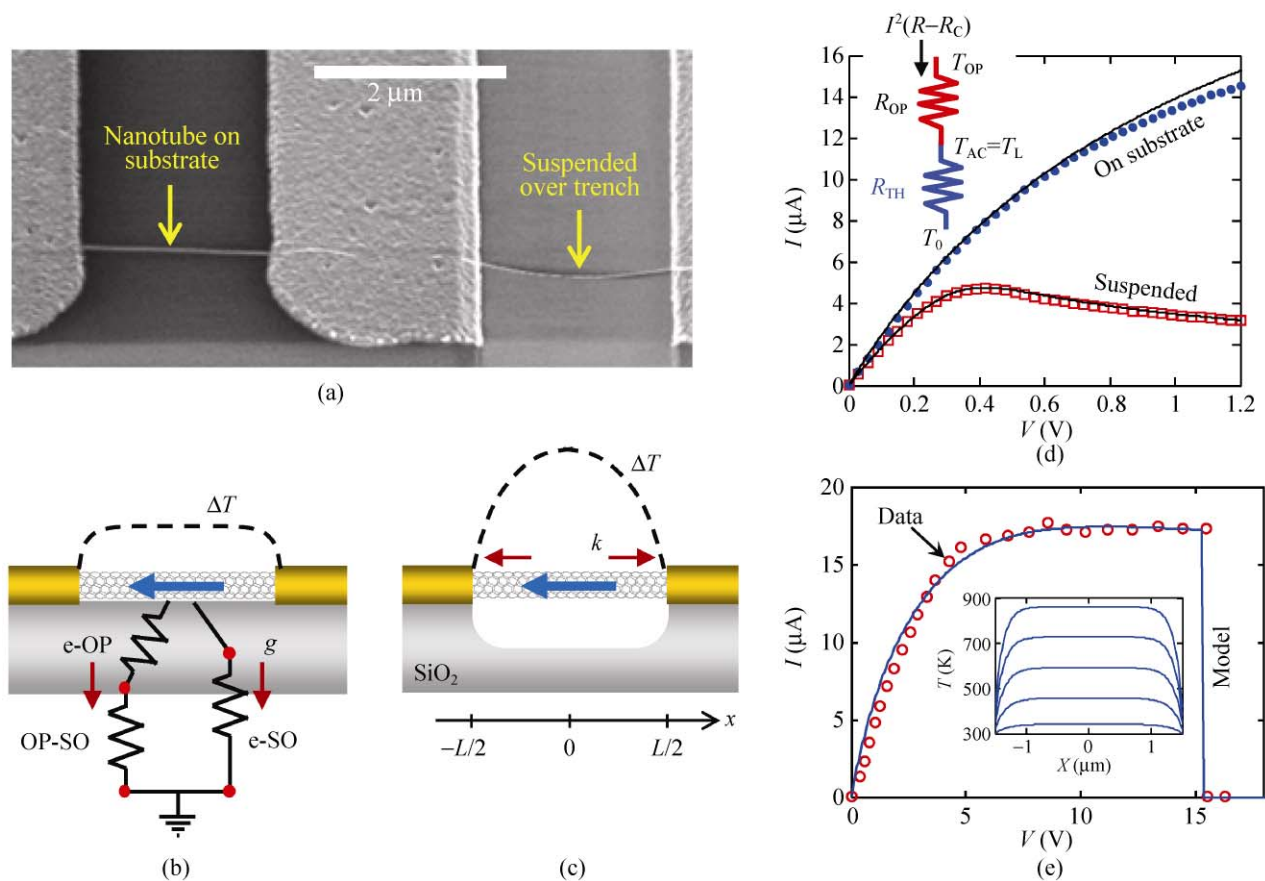

Figure 7 Energy dissipation in substrate-supported and freely suspended metallic CNTs. (a) SEM image of a single CNT that is part suspended and part supported. Reproduced with permission from Ref. [36]. Copyright 2005 American Physical Society. Schematic energy dissipation in (b) supported and (c) suspended CNTs. Red arrows show direction of heat flow. In the supported CNT, electrons scatter with device OPs, which then couple with the substrate. Electrons may also dissipate energy directly to SO phonons of the substrate [114]. (d) Measured data (symbols) and model (lines) of the CNT segments in (a). (e) Excellent agreement between data and model up to breakdown for another substrate-supported CNT ($L = 3$ μm). Inset shows the temperature profile along the CNT at applied voltages from 3 to 15 V, in 3 V increments. Reproduced with permission from Ref. [30]. Copyright 2007 American Institute of Physics

is the total electrical resistance and R_C is the combined electrical resistance of the two contacts, the temperature profile $T(x)$ of a substrate-supported metallic CNT (Fig. 7(b)) can be analytically obtained as [30, 79]:

$$T(x) = T_0 + \frac{P}{gL}\left[1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)}\right] \text{ for } -L/2 < x < L/2$$

(11)

where T_0 is the temperature of the contacts at the two ends, $L_H = (kA/g)^{1/2} \approx 0.2$ μm is the characteristic thermal length along the CNT [118], k is the thermal conductivity, and g is the net heat dissipated to the substrate per unit length. In practice, a direct measurement of this temperature profile is very challenging due to the small CNT diameter. However, a scanning thermal microscopy technique (SThM) was recently demonstrated [79], showing agreement with the "flattened" temperature profile sketched in Fig. 7(b) and obtained when the CNT length is much longer than the characteristic thermal length ($L \gg L_H$). The drawbacks of SThM on CNTs are the relatively large uncertainties in its calibration and in the temperature values obtained.

Another measurement technique that can be applied to suspended CNTs uses the temperature dependence of the Raman-active phonon G-bands [86, 119, 120]. The temperature profile of a freely suspended metallic CNT (Fig. 7(c)) is a simple inverted parabola expressed as [36]

$$T(x) = T_0 + \frac{P}{2kAL}\left[\left(\frac{L}{2}\right)^2 - x^2\right]$$

(12)

where again $-L/2 < x < L/2$ and T_0 is the temperature of the contacts at the two ends, and the power dissipation is assumed uniform along the CNT length. Analytic expressions for this temperature profile can also be obtained for a few cases of temperature-dependent thermal conductivity k [121]. The Raman-thermometry technique has directly measured this steeply varying temperature profile in suspended CNTs [119], and has confirmed the phonon non-equilibrium between optical and acoustic modes previously suggested on the basis of electrical characteristics alone (Fig. 7(d)) [36]. In the same study [119], the

authors also provided direct measurement of uneven thermal contact resistance between CNTs and their metal electrodes, with $R_{TH,L} \approx 8 \times 10^7$ K/W (left electrode) and $R_{TH,R} \approx 10^7$ K/W (right electrode) for the particular CNT under study. These are consistent with other estimates based on SThM (1.4×10^7–13.8×10^7 K/W) [79] and breakdown thermometry (~1.2×10^7 K/W) [78], but provide insight into the uneven quality of the two thermal contacts. The drawbacks of the Raman thermometry approach are its applicability to only those few CNTs resonant with the laser energy, and the relatively larger lateral resolution (~0.5 μm) compared to the SThM approach.

A third approach for substrate-supported CNTs can be referred to as "breakdown thermometry" and relies on measuring the CNT current at high voltage, including the Joule breakdown power. The voltage is gradually raised until the CNT breaks (Fig. 7(e)), while its I–V curve and breakdown power are compared to a transport model which includes heat dissipation. This was the approach adopted by Maune [77] and Pop [30, 78]. The breakdown temperature of CNTs is known to be approximately $T_{BD} \approx 600$ °C in air [122] and correlating it with the dissipated power yields the thermal coupling between CNT and substrate. This quantity is often given as a thermal conductance per CNT length, g in W·m^{-1}·K^{-1} (Eq. (11) above). The three approaches have yielded somewhat different values of CNT–SiO$_2$ thermal coupling, with SThM suggesting $g \approx 0.007$–0.06 W·m^{-1}·K^{-1} [79], Raman thermometry yielding 0.03–0.11 W·m^{-1}·K^{-1} [86], and breakdown studies giving 0.1–0.2 W·m^{-1}·K^{-1} [77, 78]. This discrepancy is not yet resolved, because the electronic contribution to thermal coupling, if any, has not yet been isolated (Fig. 7(b)), and the various measurements were made on CNTs with different diameters, substrate surface roughnesses, and ambient temperatures. For instance, breakdown thermometry yields the thermal coupling at the elevated breakdown temperatures, closer to 600 °C (although the average CNT temperature is lower). Moreover, it is relevant to point out that such nanoscale thermal coupling will be strongly dependent on the CNT diameter and substrate surface roughness of the measured samples, as recently revealed by molecular dynamics (MD) simulations [123]. The dissipation will also depend

on the substrate material itself (e.g., quartz vs. SiO$_2$) as the phonon dispersion, surface optical phonons, and interface bonding between CNTs and substrate are expected to change.

5.2 Nanowires

Unlike carbon nanotubes, nanowires are not truly one-dimensional structures. Rather, they can be thought of as shrunken three-dimensional rods which exhibit one-dimensional features (e.g., energy sub-bands) when their diameters are brought to sizes comparable to the electron or phonon wavelength (~5–10 nm). In addition, nanowire surfaces are typically very good electron and phonon scatterers, such that nanowire mobility and thermal conductivity are universally lower than the bulk mobility or thermal conductivity of the same material (Figs. 5(c), 5(d), and Fig. 8). For instance, the electrical resistivity of Cu interconnects with line widths below 100 nm increases by more than a factor of two from the bulk Cu resistivity [124], and the resistivity for line widths near 40 nm was shown to increase by at least a factor of four [125, 126] at room temperature.

The thermal conductivity of nanowires is similarly influenced by their surface. The thermal conductivity of bulk crystalline silicon is nearly 150 W·m^{-1}·K^{-1} at room temperature, which is reduced by one order of magnitude in nanowires with diameter below $D \approx 35$ nm

(Fig. 5(d) and Fig. 8(a)) [127]. In simple terms this can be understood if we express the thermal conductivity as

$$k = \frac{1}{3}Cv\lambda \simeq \frac{1}{3}\int_i C_\omega v_\omega \left(\frac{A_1}{D} + \frac{A_2}{\lambda_0} + A_3 N_i\right)^{-1} d\omega \qquad (13)$$

where C_ω is the heat capacity per unit frequency mode, v_ω is the mode velocity, λ_0 is the phonon mean free path (MFP) in the bulk material, N_i is the impurity concentration, and A_1–A_3 are fitting parameters [128–131]. The term in parenthesis represents the various contributions to the phonon MFP, including classical boundary scattering which becomes the limiting term when the diameter D falls below the range of the bulk phonon MFP, $\lambda_0 \approx 0.1$–1 µm [54]. Variations on the simple expression above have generally been successful in reproducing experimental data on thermal conductivity of silicon nanowires [127] and thin films [132].

A new twist on our understanding of thermal transport in surface-limited nanowires was presented by the recent results of Chen, Hochbaum [133, 134], and Boukai [135], who found that silicon nanowires of diameter $D < 50$ nm with very rough surfaces have thermal conductivity *one hundred* times lower than that of bulk crystalline silicon (Fig. 8(b)). This approaches the thermal conductivity of amorphous silicon, and cannot be understood on the basis of classical boundary scattering alone (the $1/D$ term in Eq. (13)). To explain it, Martin et al. [131] proposed an additional
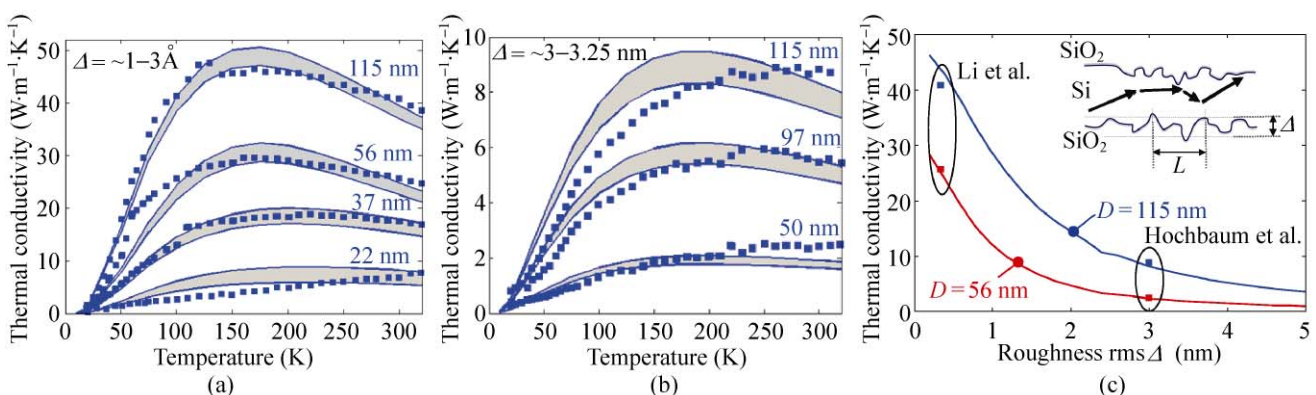

Figure 8 Measured (symbols) and modeled (lines) thermal conductivity of silicon nanowires (NWs) with various diameters D. (a) Thermal conductivity of smooth-surface NWs. Shaded areas correspond to surface roughness parameter $\Delta = 1$–3 Å. (b) Thermal conductivity of rough-surface NWs. Shaded areas correspond to $\Delta = 3.00$–3.25 nm. (c) Strong dependence of thermal conductivity on surface roughness Δ at room temperature. Inset shows a schematic of the nanowire cross-section. Experimental data from Ref. [127, 133], modeling described in Ref. [131]. Reproduced with permission. Copyright 2009 American Physical Society.

scattering term which relies on a description of the surface through a roughness height Δ and auto-covariance length L (Fig. 8(c)). This accounts for the fact that phonons "see" the rough nanowire as a series of constrictions along their propagation direction. Unlike classical boundary scattering, the roughness scattering rate is strongly frequency dependent (~ω^2), with little impact on long-wavelength phonons. Using a full phonon dispersion for silicon, Martin et al. [131] found an approximately quadratic dependence of nanowire thermal conductivity on diameter and roughness as $(D/\Delta)^2$. While the exact surface roughness in the experiments is difficult to measure, it appears that the enhanced model does predict a very strong role for it, particularly for smaller diameter nanowires (Figs. 8(b) and 8(c)). If the electrical conductivity can be preserved, arrays of such nanostructures could form efficient thermoelectric devices, a domain of ongoing investigations.

6. Thermal rectification

In addition to impeding or enhancing electrical and thermal transport, nanoscale structuring could also be used to introduce thermal flow asymmetry. This is the thermal equivalent of the electrical p–n diode, a two-terminal device that achieves greater heat flux in one direction than another, e.g., $Q_{BA} > Q_{AB}$ for the same temperature difference ΔT, where A and B are its two terminals (Fig. 9) [136]. Thus, we can define the rectification ratio $\gamma = Q_{BA}/Q_{AB} > 1$ which will be referred to below. In the context of electronics and systems, thermal rectifiers could enable thermal flow to be processed independently from electron current, or suggest the possibility of phononic devices and thermal logic [137]. In the context of heat engines or buildings, such thermal rectifiers could act as energy harvesting materials, exploiting naturally occurring temperature gradients with the environment.

A certain amount of thermal rectification can be achieved between two bulk materials with strongly different thermal conductivity dependence on temperature [138]. This is in fact a classical Fourier law effect, first observed in the 1970s [139, 140] and recently reexamined by Dames [138] and Kobayashi et al. [141]. As shown in Fig. 9(a), the two sides of the junction require two materials with strongly decreasing
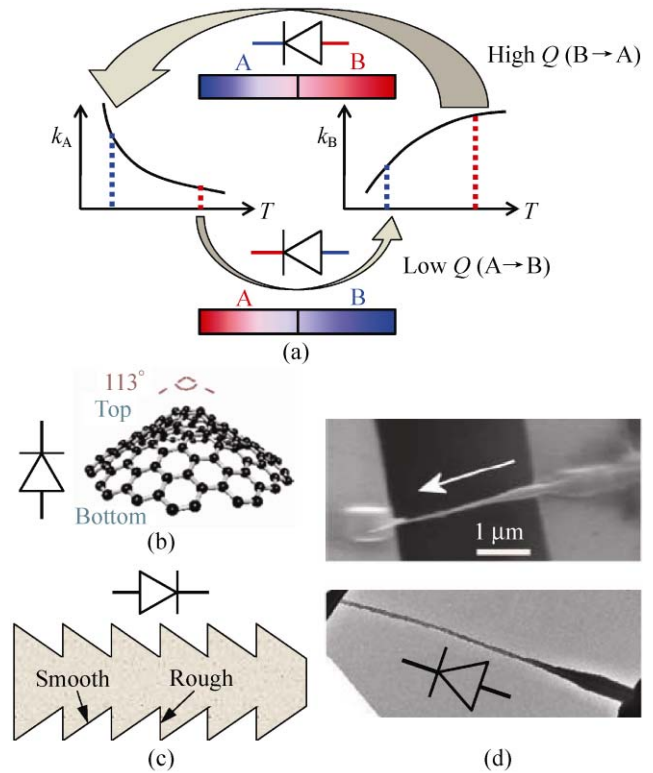

Figure 9 Thermal rectification concepts, the thermal equivalent of a p–n diode. (a) Asymmetric heat flow can be achieved between two bulk materials with different temperature dependence of thermal conductivity [138, 141]. Some proposed theoretical concepts rely on phonon filtering or bottlenecks induced by asymmetric geometry, e.g., (b) carbon nanocone. (Reproduced with permission from Ref. [142]. Copyright 2008 American Physical Society.) or (c) sawtooth nanowire [144]. (d) In practice, the only nano-structured thermal rectifier has been achieved with asymmetrically mass-loaded carbon (top) and boron nitride (bottom) nanotubes. The diode symbol illustrates the rectification direction. Reproduced with permission from Ref. [145]. Copyright 2006 AAAS.

(A) and increasing (B) temperature dependence of thermal conductivity. When B is the "hot" and A is the "cold" terminal ($\Delta T = T_B - T_A$), both materials are in a regime of high thermal conductivity, and heat flows more easily from B to A (top, wider arrow in Fig. 9(a)). When the terminals are reversed ($\Delta T = T_A - T_B$), both materials are in a regime of lower thermal conductivity, and heat flow is reduced between A and B (bottom, thinner arrow). This leads to an asymmetric heat flux, $Q_{BA} > Q_{AB}$ for the same temperature difference ΔT. Such thermal rectification was recently observed by Kobayashi et al. [141], who noted a heat flux ratio $\gamma \approx 1.43$ between $LaCoO_3$ and $La_{0.7}Sr_{0.3}CoO_3$ in the temperature range 70–100 K.

Suggestions of nanostructures for thermal rectification have only appeared in the past few years. Several theoretical proposals [142, 143] have been put forward, estimating thermal rectification as high as $\gamma \approx 100$–1000 between two directions. Thermal rectification could be achieved through nanoscale structuring, e.g., inducing nano-indentations that preferentially scatter phonons [144], through geometrical heat "funneling", e.g., in the case of a carbon nanocone [142], or by asymmetric mass-loading [145], as illustrated in Figs. 9(b)–9(d). Most suggestions based on nanoscale thermal rectification have been purely theoretical, requiring engineering of coupling and layout between individual atoms, which are very difficult to achieve in practice. The only nanoscale thermal rectifier demonstrated to date at room temperature [145] has shown thermal rectification ratios $\gamma \approx 1.02$–1.07. This device relied on suspended, several microns-long multi-walled carbon or boron nitride nanotubes that were unevenly mass-loaded with a much heavier molecular species, trimethyl(methylcylopentadienyl)platinum $(C_9H_{16}Pt)$, (Fig. 9(d)). In this case, heat flow preference was from the high- to the low-mass regions of the loaded nanotube. Thermal rectification at very low-temperature (0.08 K) and high magnetic field (10 T) has also been demonstrated in single quantum dots, with heat flow asymmetry $\gamma \approx 1.11$ [146]. Clearly, much work remains to be done to achieve a practical, room-temperature thermal diode with rectification up to theoretically-predicted ($\gamma \approx 100$–1000) limits.

7. Interfaces

Nanoscale one- and two-dimensional devices have very little "bulk" and thus their behavior is strongly dominated by their interfaces in terms of energy transport and dissipation. This is particularly evident for thermal conductivity in nanowires, or thermal dissipation in nanotubes, as outlined above. While the experimental data and theoretical understanding of nanoscale device interfaces are just beginning to take shape, a wealth of experimental data exists for energy transport across interfaces between otherwise bulk solids. This is summarized in Fig. 10. The interface thermal conductance relates the heat flux Q crossing an interface to the temperature drop ΔT at

the interface, $Q = G\Delta T$. Thermal interfaces are most often studied with pump-probe optical techniques such as time-domain thermoreflectance (TDTR), picosecond transient absorption [147–152], or the 3-omega method [153–157]. As summarized in Fig. 10, these studies have shown that the thermal conductance of bulk solid interfaces at room temperature spans a relatively limited range, but depends on composition of the interface at the level of a single molecular layer [158].

The range of available thermal conductances at material interfaces appears to approach two limits. At
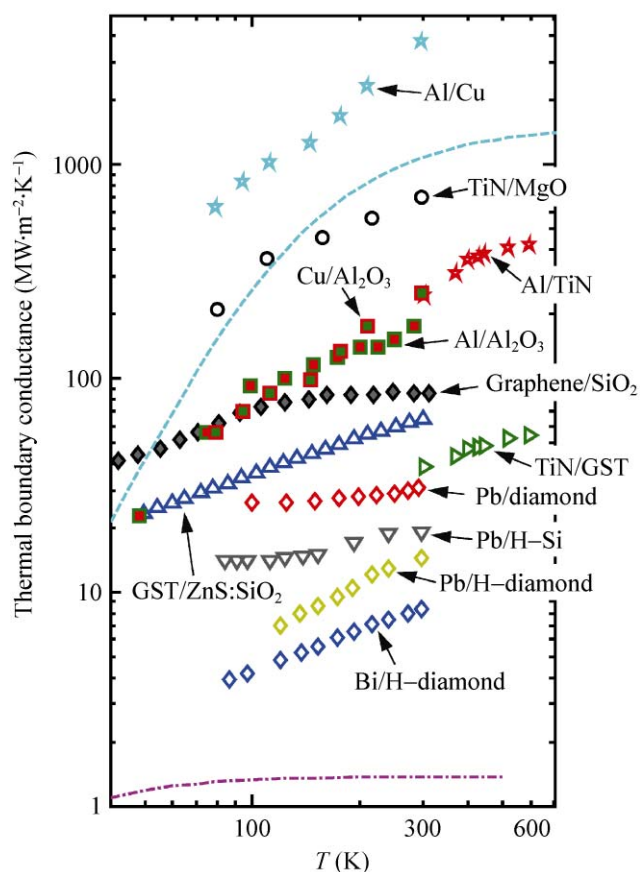

Figure 10 Thermal conductance of various material interfaces, compiled from Refs. [90, 148, 149, 157, 159, 166, 167] [GST = $Ge_2Sb_2Te_5$]. The dashed upper line is a diffuse-mismatch model calculation of the TiN/MgO interface [148], the dashed lower line is the radiation limit for the Bi/H–diamond interface [149]. The highest known conductance is at good metal interfaces (Al/Cu) where electrons dominate the thermal exchange [159]. The lowest known conductance is between materials with highly mismatched phonon modes and Debye temperatures (Bi/H–diamond) [149]. Compared to other properties of materials, the thermal conductance of solid material interfaces spans a relatively modest range ($\sim$500$\times$), and most interfaces fall in the range 10–100 MW·m^{-2}·K^{-1} at room temperature

the upper end, the best measured thermal interfaces are between metals with good intrinsic thermal properties, e.g., Al/Cu. Thermal transport across these interfaces appears to be mediated by electrons, and the phonon contribution is less than 10% [159]. The best metal-dielectric thermal interfaces occur between materials with similar Debye temperatures Θ_D (such as highly annealed, epitaxial TiN on single crystal oxides [148]) and approach the limit of a phonon diffuse mismatch model (DMM) [160]. At the low end, a large Debye temperature mismatch between the two materials is expected to lead to significant thermal impedance, such as between Pb or Bi ($\Theta_D \approx$ 110 K) and diamond ($\Theta_D \approx 2200$ K) [149]. The Debye temperature is a typical figure of merit for the differences in vibrational spectrum and the phonon density of states between the two sides of the interface. With regard to Fig. 10, it is interesting to note the physical meaning of the thermal interface conductance by relating it to the equivalent thermal impedance of a dielectric layer with thickness d and thermal conductivity k, i.e., $G = k/d$. Thus, an interface with $G = 10$ MW·m^{-2}·K^{-1} is equivalent to the thermal impedance of a 140 nm film of SiO$_2$ ($k_{ox} = 1.4$ W·m^{-1}·K^{-1}) and $G = 100$ MW·m^{-2}·K^{-1} is equivalent to the thermal impedance of 14 nm of SiO$_2$. This simple comparison also highlights the importance of such material interfaces in all nanometer scale devices and structures.

Among one- or two-dimensional conductors, some of the available data on interface thermal resistance for carbon nanotubes were already presented in Section 5.1, and data for the graphene/SiO$_2$ thermal interface are shown in Fig. 10. In particular, given the comparable Debye temperature of CNTs and graphene with that of diamond, one expects a significant vibrational mismatch between them and other materials with typically lower Θ_D. To compare the data available for CNTs with that of other material interfaces, the range of thermal conductance per unit length $g \approx 0.007$–0.2 W·m^{-1}·K^{-1} [77–79, 86] can be converted to $G \approx 4$–100 MW·m^{-2}·K^{-1} per unit area when normalized by a 2 nm CNT diameter, well within the range of the experimental data in Fig. 10. In particular, given the large intrinsic thermal conductivity of CNTs it appears that their thermal resistance is nearly always dominated by their interface with the environment, both for solid [151] as well as liquid composites [150]. Nevertheless, little is yet known about how to engineer one-dimensional interfaces between dissimilar materials such as CNTs and their dielectric environments, and much work remains to be done in this area.

8. Conclusions

Understanding and controlling energy dissipation and transport in nanostructures will continue to be an area of rapid improvement and discovery, with applications ranging from low-power electronics to energy-efficient data centers, and thermal energy harvesting. For instance, reducing power dissipation in electronics will impact a wide range of applications from portable devices (10^{-3} W) to massive data centers (10^9 W). Such developments would also improve weight payloads for mobile electronics and medical instrumentation (fewer heavy batteries), and potentially exploit ubiquitous thermal gradients—from sources as varied as car engines, power plants, or even body-environment temperature differences—as supplies of electrical energy.

On a large scale, by simple estimates even a transistor twice as energy-efficient could lower nationwide power use by over 10^{10} W if implemented today, which is a significant percentage of our national power budget. Given that energy use by electronics is on a trend that could reach 30% of the national electricity consumption by 2025, such progress is crucial to maintaining progress in a post-CMOS world, and has great environmental implications as well. In addition, just over half the world energy is wasted as heat (~10^{13} W), from nuclear power plants and factories to car engines and the power bricks on our laptops. Efficiently reclaiming even a small percentage of such wasted heat would itself nearly satisfy the electricity needs of our planet.

Acknowledgements

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